What is claimed is:

1. A semiconductor memory device operating in synchronization with an external clock, comprising:

a frequency-detecting unit that receives the external clock, detects clock frequency information of the external clock, and outputs the detected clock frequency information; and

a duty cycle correction circuit that corrects the duty cycle of the external clock in response to the clock frequency information.

2. The semiconductor memory device of claim 1, wherein the duty cycle correction circuit comprises:

a first delay locked loop that receives the external clock, inverts and delays the external clock, synchronizes the delayed external clock with the inverted external clock, and outputs the delayed synchronized external clock;

a second delay locked loop that receives and delays the inverted external clock, synchronizes the delayed inverted external clock with the external clock, and outputs the delayed synchronized inverted clock; and

an interpolation circuit which interpolates a signal inverting the output signal of the first delay locked loop with the output signal of the second delay locked loop, and outputs the interpolated signal.

3. The semiconductor memory device of claim 2, wherein the interpolation circuit comprises:

a first inverting circuit that receives the signal inverting the output signal of the first delay locked loop, inverts the received signal, and outputs the inverted signal;

a second inverting circuit that inverts the output signal of the second delay locked loop and outputs the inverted signal, the output end of the first inverting circuit and the output end of the second inverting circuit connected with each other;

a third inverting circuit that receives and inverts the output signal of the first inverting circuit and the output signal of the second inverting circuit, and outputs the inverted signal; and

a plurality of capacitors having predetermined capacitances, connected between a ground power supply and respective input ends of the first, second, and third inverting circuits,

wherein the capacitances of the plurality of capacitors are controlled by the clock frequency information.

4. The semiconductor memory device of claim 3, wherein when the clock frequency of the external clock is high, the capacitances of the plurality of capacitors are small, and when the clock frequency of the external clock is low, the capacitances of the plurality of capacitors are large.

5. The semiconductor memory device of claim 1, wherein the frequency detecting unit comprises:

a frequency detecting circuit that receives the external clock and detects the clock frequency of the external clock;

an analog-to-digital converter (ADC) that receives an output signal of the frequency detecting circuit, converts the output signal into a digital signal, and outputs the digital signal; and

a register that receives the output signal of the ADC and stores the output signal of the ADC as the clock frequency information.

6. A semiconductor memory device operating in synchronization with an external clock, comprising

a duty cycle correction circuit that receives the external clock, corrects the duty cycle of the external clock, and outputs the corrected duty cycle, wherein the duty cycle correction circuit comprises:

a first delay locked loop that receives the external clock, inverts and delays the external clock, synchronizes the delayed external clock with the inverted external clock, and outputs the delayed synchronized external clock;

a second delay locked loop that receives and delays the inverted external clock, synchronizes the delayed inverted external clock with the external clock, and outputs the delayed synchronized inverted clock;

an inverting circuit that inverts the output signal of the first delay locked loop;

an interpolation circuit that interpolates the output signal of the inverting circuit with the output signal of the second delay locked loop and outputs an interpolated signal; and

a control circuit that controls the interpolation circuit in response to clock frequency information for the external clock.

7. The semiconductor memory device of clam 6, wherein the control circuit generates the clock frequency information by measuring the frequency of the external clock.

8. The semiconductor memory device of claim 6, wherein the control circuit bases the clock frequency information on CAS (column address strobe) latency.

9. A semiconductor memory device operating in synchronization with an external clock, comprising:

a first delay locked loop that receives the external clock, inverts and delays the external clock, synchronizes the delayed external clock with the inverted external clock, and outputs the delayed synchronized external clock;

a second delay locked loop that receives and delays the inverted external clock, synchronizes the delayed inverted external clock with the external clock, and outputs the delayed synchronized inverted clock; and

an interpolation circuit that interpolates a signal inverting the output signal of the first delay locked loop with the output signal of the second delay locked loop and outputs the interpolated signal,

wherein the interpolation circuit is controlled by CAS (column address strobe) latency.

10. The semiconductor memory device of claim 9, wherein the interpolation circuit comprises:

a first inverting circuit that receives and inverts the signal inverting the output signal of the first delay locked loop and outputs the inverted signal;

a second inverting circuit that inverts the output signal of the second delay locked loop and outputs the inverted signal, the output end of the first inverting circuit and the output end of the second inverting circuit being connected with each other;

a third inverting circuit that receives the output signal of the first inverting circuit and the output signal of the second inverting circuit, inverts these signals, and outputs the inverted signals; and

a plurality of capacitors having predetermined capacitances connected between a ground power supply and respective input ends of the first, second, and third inverting circuits,

wherein the capacitances of the plurality of capacitors are controlled by the CAS latency.

11. The semiconductor memory device of claim 10, wherein when the clock frequency of the external clock is high, the capacitances of the plurality of capacitors are small, and when the clock frequency of the external clock is low, the capacitances of the plurality of capacitors are large.

12. An interpolation circuit, included in a semiconductor memory device, that interpolates two clock signals whose clock frequencies identify with each other and whose phases are different from each other, the interpolation circuit comprising:

a first inverting circuit that receives a first clock signal having a predetermined clock frequency, inverts the first clock signal, and outputs the inverted first clock signal;

a second inverting circuit that receives a second clock signal having a predetermined clock frequency, inverts the second clock signal, and outputs the inverted second clock signal, the output end of the first inverting circuit and the output end of the second inverting circuit being connected with each other;

a third inverting circuit that receives and inverts the output of the first inverting circuit and the output of the second inverting circuit and outputs the inverted signals; and

first, second, and third capacitors having predetermined capacitances, connected between a ground power supply and respective input ends of the first, second, and third inverting circuits,

wherein the capacitances of the first, second, and third capacitors are controlled according to the clock frequency.

13. The interpolation circuit of claim 12, wherein when the clock frequency of the external clock is high, the capacitances of the first, second, and third capacitors are small, and

when the clock frequency of the external clock is low, the capacitances of the first, second, and third of capacitors are large.

14. The interpolation circuit of claim 12, wherein the capacitances of the first, second, and third of capacitors are controlled by CAS latency of the semiconductor memory device.

15. The interpolation circuit of claim 14, wherein when the CAS latency is high, the capacitances of the first, second, and third capacitors are small, and when the CAS latency is low, the capacitances of the first, second, and third of capacitors are large.